REMARKS

Claims 1-10 and 19-30 are pending in this application, of which claims 1-2 and 6 have been amended and claims 22-30 are newly-added.

In view of the aforementioned amendments and accompanying remarks, claims 1-10 and 19-30, as amended, are in condition for further examination.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made
RCE
Amendment Transmittal

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/855,590

IN THE CLAIMS:

Please amend claims 1-2 and 6 as follows:

1. (Twice Amended) A semiconductor device having a multiple layer wiring structure that is provided with two or more metal layers and having a stack VIA portion [in which, when] for connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, [wherein the semiconductor device having a multiple layer wiring structure comprises:] comprising:

two or more partitioned intermediate metal layers that are partitioned inside the connection area; and

an intermediate metal layer wiring area that is sandwiched by the partitioned intermediate metal layers.

2. (Twice Amended) The semiconductor device according to claim 1, wherein the connection metal layer and the layer to be connected intersect in [a] the connection area.

6. (Amended) The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the partitioned intermediate metal layers are formed in accordance with minimum design rules in a [transverse] direction that is orthogonal to the priority wiring

direction of the intermediate metal layer.